IN THE CLAIMS

Please cancel without prejudice claims 31-60.

1. (Previously Presented) A method comprising:

receiving at an IO controller hub an interrupt from an IO device;

the IO controller hub converting said interrupt into an upstream memory write interrupt by generating a memory write request to a predetermined address of a memory space, the memory write request being processed via one or more memory cycles by a memory controller hub; and

the memory controller hub converting said upstream memory write interrupt into a front side bus (FSB) interrupt transaction, wherein one or more processors coupled to the FSB are capable of receiving the FSB interrupt as a part of a FSB transaction.

2. (Original) The method as in claim 1, wherein said interrupt is generated by a peripheral component interconnect (PCI) device.

3. (Original) The method as in claim 2, wherein said FSB interrupt is received by a processor.

4. (Previously Presented) A method comprising:

receiving at an IO controller hub a message signaled interrupt (MSI) interrupt;

IO controller hub forwarding said MSI interrupt to a memory controller via a memory write request addressed to a predetermined address of a memory space, the memory write request being processed via one or more memory cycles; and

The memory controller converting said MSI interrupt into an FSB interrupt transaction, wherein one or more processors coupled to the FSB are capable of receiving the FSB interrupt as a part of a FSB transaction.

5. (Original) The method as in claim 4, wherein said MSI interrupt is generated by a PCI device, and wherein said FSB interrupt is received by a processor.

6. (Original) The method as in claim 5, wherein said FSB interrupt is received by a processor.

7. (Previously Presented) A method comprising:

receiving a hardware signal by an IO controller hub, the hardware signal being generated from a hardware interrupt;

the IO controller hub converting said hardware signal into an upstream memory write interrupt via a memory write request addressed to a predetermined address of a memory space, the memory write request being processed via one or more memory cycles by a memory controller hub; and

the memory controller hub converting said upstream memory write interrupt into an FSB interrupt transaction, wherein one or more processors coupled to the FSB are capable of receiving the FSB interrupt as a part of a FSB transaction.

8. (Original) The method as in claim 7, wherein said hardware signal is generated by a PCI device, and wherein said FSB interrupt is received by a processor.

9. (Original) The method as in claim 8, wherein said FSB interrupt is received by a processor.

10. (Previously Presented) An apparatus comprising:

a chipset, an IO controller hub (ICH) configured to receive an interrupt from at least one I/O (input and output) device[[,]] and to convert said interrupt into an upstream memory write interrupt processed as one or more memory cycles[[,]] ; and

a memory controller hub (MCH) configured to convert said upstream memory write interrupt into an FSB interrupt transaction, which is processed on a FSB (front side bus).

11. (Previously Presented) The apparatus as in claim 10, said chipset further comprising at least one of an I/O controller hub (ICH), P64H, AGP device.

12. (Previously Presented) The apparatus as in claim 11, further comprising an I/O component of an advanced programmable interrupt controller (IOxAPIC) configured to convert said interrupt into said upstream memory write interrupt.

13. (Previously Presented) The apparatus as in claim 12, said chipset further comprising a HUB interface coupled on having a first end coupled to said IOxAPIC and coupled on a second end coupled to a MCH, wherein said memory controller hub (MCH) configured to convert said upstream memory write interrupt into said FSB interrupt transaction.

14. (Original) The apparatus as in claim 10, wherein said interrupt is generated by a PCI device, and wherein said chipset is coupled to a processor.

15. (Original) The apparatus as in claim 10, wherein said interrupt is a MSI interrupt.

16. (Previously Presented) The apparatus as in claim 15, said chipset further comprising a HUB interface coupled on having a first end coupled to an ICH and coupled on a second end coupled to a MCH, wherein said ICH configured to forward said MSI interrupt to said HUB interface, and wherein said MCH configured to convert said MSI interrupt into a FSB interrupt transaction.

17. (Original) The apparatus as in claim 16, wherein said MCH configured to ensure at least one data pipe of a HUB interface is flushed upstream before propagating an interrupt upstream.

18. (Original) The apparatus as in claim 16, wherein said MCH configured to receive an end of interrupt (EOI) from a processor and broadcast said EOI to at least one downstream HUB interface IOxAPIC generating at least one level mode interrupt.

19. – 60. (Canceled)